REMARKS

This is in response to the Office Action of 01 November 2005. Claims 1-4 are pending in the application, and Claims 1 and 3 have been amended in a non-narrowing manner. New Claims 5-10 have been added, By this Response and Amendment, independent Claims 1 and 3 have been amended in a non-narrowing manner, new Claims 5-10 have been added, and arguments traversing the rejections are presented.

No new matter has been added.

In view of the amendments above and remarks below, Applicant respectfully requests reconsideration and further examination.

About The Invention

The present invention relates generally to ESD protection circuits, and more particularly to reducing the capacitive loading on input terminals. Various embodiments of the present invention provide an ESD protection circuit having one diode, rather than the conventionally provided two parallel diodes configured in opposition. In accordance with the present invention, a parasitic diode in a rectifier circuit is shared with the ESD protection circuit to provide the desired ESD protection function, while reducing the loading on the input terminals as compared to conventional ESD protection circuits.

Rejections under 35 USC §103(a)

Claims 1 and 3 have been rejected under 35 USC §103(a) as being unpatentable over acknowledged prior art in view of Duvvury, et al., (US Patent 5,493,133). Claims 2 and 4 have been rejected under 35 USC §103(a) as being unpatentable over acknowledged prior art in view of Duvvury, et al., and further in view of Ellis (US Patent 5,550,728).

Applicant respectfully traverses the rejections of Claims 1-4 and requests that these rejections be withdrawn. Applicant presents below, a discussion of the

disclosure of Duvvury, et al., and shows that the invention defined by the Claims is neither disclosed, suggested, or motivated by the references.

Duvvury, et al., disclose a protection circuit, and physical layout, providing both positive and negative stress protection and which is compatible to +/-20 V operation. The positive stress protection of Duvvury, et al., is provided by a PNP punchthrough-assisted silicon-controlled-rectifier (SCR) and the negative stress protection is provided by a vertical [illegible] rectifier", is not the same as a "rectifier circuit" which is used to provide a power supply voltage, as is described by Applicant. As can be seen in Fig. 2 of Duvvury, et al., n-well 44 is nominally floating. Duvvury, et al., disclose that a Schottky diode can be used to provide a bias voltage to n-well 44 so as to reduce or prevent a CMOS latch-up phenomenon.

Applicant's invention is directed to an ESD protection circuit which reduces the input loading by including one, rather than two, p/n diodes. The required electrostatic discharge protection functionality is achieved in embodiments of the present invention by combining the reduced load, one diode, ESD circuit, with a rectifier circuit containing a parasitic p/n junction diode, such that the parasitic p/n junction is coupled to be shared with the ESD circuit and provide the two-diode protection configuration. The Claims recite that the parasitic p/n junction diode is a part of a Schottky diode of the rectifier circuit.

Independent Claims 1 and 3 have been amended in a non-narrowing manner. More particularly, no limitations have been added, but rather the wording has been changed to improve readability. These amendments to Claims 1 and 3 make clear that the ESD protection circuit has one diode included therein, and a rectifier circuit, which is connected to the ESD circuit, includes a parasitic diode which is shared with the ESD circuit such that the ESD circuit and the rectifier circuit taken together, provide the two parallel diodes needed for provided electrostatic discharge protection.

As indicated above, there are differences between the teachings of Duvvury, et al., and the invention defined by the Claims. The claimed invention

does not include the PNP/NPN bipolar arrangement of Duvvury, et al. The [illegible] circuit, which includes a Schottky diode, to be coupled to the ESD circuit, and further requires that there be a parasitic p/n junction diode associated with the Schottky diode. It is this parasitic p/n junction diode, which when coupled with the one diode of the ESD circuit, provides the required ESD protection. Duvvury, et al., do not describe a parasitic p/n junction in a rectifier circuit that is shared with an ESD circuit. In fact, Duvvury, et al., describe the fabrication of their Schottky diode without disclosing any such parasitic structure ("Schottky diode 64 may comprise a metal such as platinum (not shown) directly adjacent the surface of n-well 44.").

Duvvury, et al., do not disclose, suggest, or provide motivation for the invention set forth in independent Claims 1 and 3.

In view of the foregoing, Applicant respectfully submits that the rejection of independent Claims 1 and 3, and the Claims that depend therefrom, is improper, and should be withdrawn.

New Claims 5-6

New Claims 5-6 are directed to an integrated circuit that embodies the present invention in which a rectifier circuit includes a parasitic diode that is shared with an ESD protection circuit so as to complete the ESD protection circuit. Support for Claims 5-6 can generally be found throughout the specification, and can more particularly be found in the specification at pages 5-6, and in Figs. 2 and 3.

Conclusion

All of the rejections in the outstanding Office Action of 01 November 2005 have been responded to, and Applicant respectfully submits that the pending Claims 1-6 are now in condition for allowance.

Appl. No. 10/517,327

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By _____

Dated: 00 January 0000
Hillsboro, Oregon

Reg. No. 34,752